MY-Semi

Preliminary

MY9868A

16-Channel Constant Current LED Driver With Double Latch Technology

General Description

The MY9868A, 16-channel constant current LED driver with double latch display technology, is suitable for any static and dynamic applications. The distinctive double latch technology enhances the visual refresh rate and low grayscale uniformity by increasing LED utilization rate. And the ghost image abatement is designed to eliminate ghosting of multiplexing LED modules due to parasitic capacitors.

The device operates over a 3.3V to 5V input voltage range (±10%) and provides 16 open-drain constant current sinking outputs that are rated to 17V and delivers up to 45mA of high accuracy current to each string of LED. The current at each output is programmable by means of an external current-sensing resistor.

The MY9868A's on-board pass elements minimize the need for external components, while at the same time, providing ±3% channel current accuracy and ±4% chip current accuracy. Additional features include a ±0.1% regulated output current capability.
The MY9868A is available in a 24-pin SSOP/QFN package and specified over the -40℃ to +85℃ ambient temperature range.

Features

- 3.3V ~ 5.0V Operating supply voltage (±10%)
- 5~45mA/5V Constant current output range
- 5~30mA/3.3V Constant current output range
- 17V Rated output channels for long LED strings
- ±3% (max.) Current accuracy between channels
- ±4% (max.) Current accuracy between chips
- ±0.1% Output current regulation capability
- Double latch display technology (Patent approved)
- Visual refresh rate, LED utilization rate, grayscale level and low brightness uniformity are better than conventional pure drivers
- Current setting by one external resister
- Ghost image abatement
- High HBM ESD protection (Iout pin > 8000V)
- -40℃ to +85℃ Ambient temperature range

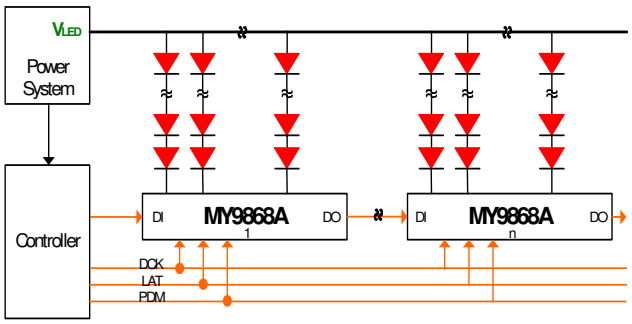
Applications

- Indoor and Outdoor LED Video Displays
- Variable Message Sign (VMS)
- Dot Matrix Module
- Architectural and Decorative Lighting
- Industrial Lighting
- LCD Display Backlighting

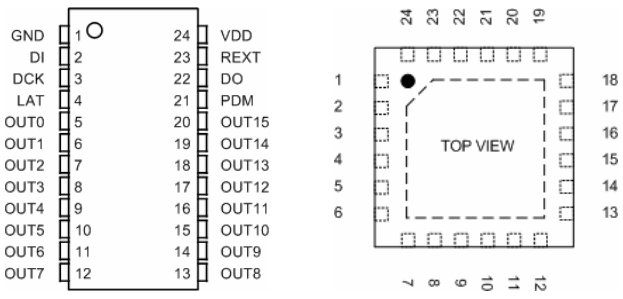
Order information

Part	Package Information	
MY9868ASS	SSOP24-150mil-0.635mm	2500 pcs/Reel
MY9868AQF	QFN24-4mmx4mm-0.5mm	3000 pcs/Reel
MY9868AQA	QFN24-4mmx4mm-0.5mm	3000 pcs/Reel

Typical Operating Circuits

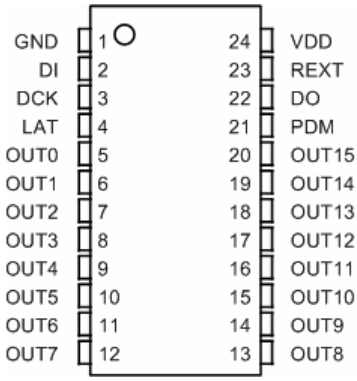


Pin Configuration

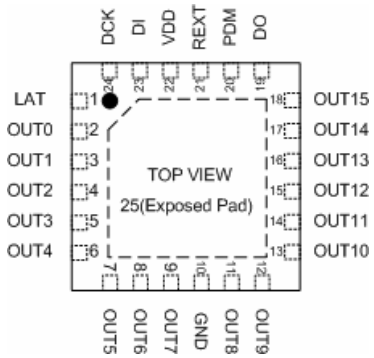


For pricing, delivery, and ordering information, pleases contact MY-Semi Inc. at +886-3-560-1668, or email to INFO@MY-Semi.com.tw or visit MY-Semi's website at www.MY-Semi.com.tw

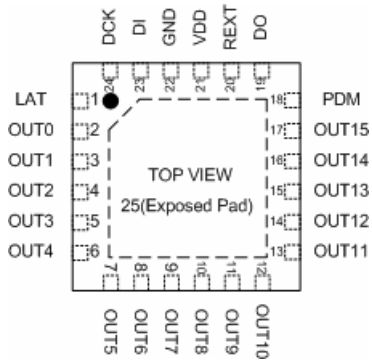
Pin Description



MY9868A SS



MY9868A QF

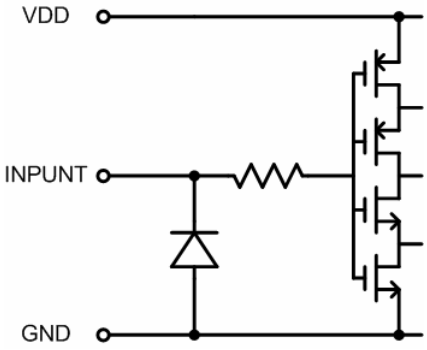


MY9868A QA

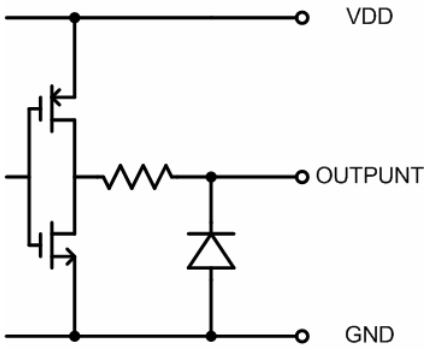
PIN No.			PIN NAME	FUNCTION
SS	QF	QA		
1	10,25	22,25	GND	Ground terminal.
2	23	23	DI	Serial data input terminal.
3	24	24	DCK	Synchronous clock input terminal for serial data transfer.
4	1	1	LAT	Input terminal of data strobe.
5~20	2~9,11~18	2~17	OUT0~15	Sink constant-current outputs (open-drain).
21	20	18	PDM	Grayscale Modulation Input terminal:
22	19	19	DO	Serial data output terminal.
23	21	20	REXT	External resistors connected between REXT and GND for output current value setting.
24	22	21	VDD	Supply voltage terminal.

Equivalent Circuit of Inputs and Output

1. DCK, DI, LAT, PDM terminals



2. DO terminal



Maximum Ratings (Ta=25°C, Tj(max) = 150°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VDD	-0.3 ~ 7.0	V
Input Voltage	VIN	-0.3 ~ VDD+0.3	V
Output Current	IOUT	45	mA
Output Voltage	VOUT	-0.3 ~ 17	V
Input Clock Frequency	FDCK	30	MHz
GND Terminal Current	IGND	800	mA
Thermal Resistance (On PCB)	Rth(j-a)	70.5 (SS:SSOP-150mil-0.635mm)	°C/W
		36.9 (QT/QE:QFN24-4mmx4mm)	
Operating Supply Voltage	VDD	3.3 ~ 5.0 (±10%)	V
Operating Ambient Temperature	Top	-40 ~ 85	°C
Storage Temperature	Tstg	-55 ~ 150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only and functional operation of the device at these or any other condition beyond those specified is not supported.
(2) All voltage values are with respect to ground terminal.

Electrical Characteristics (VDD = 5.0 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage "H" Level	VIH	CMOS logic level	0.7VDD	—	VDD	V
Input Voltage "L" Level	VIL	CMOS logic level	GND	—	0.3VDD	
Output Leakage Current	ILK	VOUT = 17 V	—	—	0.1	uA
Output Voltage (DO)	VOL	IOL = 1 mA	—	—	0.4	V
	VOH	IOH= 1 mA	VDD-0.4	—	—	
Output Current Skew (Channel-to-Channel) *1	dIOUT1	VOUT = 1.0 V Rrext = 0.94 KΩ	—	±1.0	±3.0	%
Output Current Skew (Chip-to-Chip) *2	dIOUT2		—	±1.0	±3.0	%
Output Current Skew (Channel-to-Channel)*1	dIOUT3	VOUT = 1.0 V Rrext = 3.69 KΩ	—	±1.5	±3.0	%
Output Current Skew (Chip-to-Chip)*2	dIOUT4		—	±1.5	±4.0	%
Output Voltage Regulation*3	% / VOUT	Rrext = 0.94 KΩ VOUT = 1 V ~ 3 V	—	±.0.1	—	% / V
Supply Voltage Regulation*4	% / VDD	Rrext = 0.94 KΩ VDD = 3 V ~ 5.5 V	—	±0.6	±1	
Supply Current *5	$I_{DD1(off)}$	input signal is static Rrext = 3.69 KΩ all outputs turn off	—	1.6	—	
	$I_{DD2(on)}$	input signal is static Rrext = 3.69 KΩ all outputs turn on	—	2.5	—	
	$I_{DD3(off)}$	input signal is static Rrext = 0.94 KΩ all outputs turn off	—	4.5	—	
	$I_{DD4(on)}$	input signal is static Rrext = 0.94 KΩ all outputs turn on	—	5.5	—	

*1 Channel-to-channel skew is defined by the formula below:

$$\Delta(\%) = \left[\frac{Iout_n}{\frac{(Iout_0 + Iout_1 + ... + Iout_{15})}{16}} - 1 \right] * 100\%$$

*2 Chip-to-Chip skew is defined by the formula below:

$$\Delta(\%) = \left[\left(\frac{\frac{(Iout_0 + Iout_1 + ... + Iout_{15})}{16} - (Ideal\ \ Output\ \ Current)}{(Ideal\ \ Output\ \ Current)} \right) \right] * 100\%$$

*3 Output voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[\frac{Iout_n(@Vout_n = 3V) - Iout_n(@Vout_n = 1V)}{Iout_n(@Vout_n = 3V)} \right] * \frac{100\%}{3V - 1V}$$

*4 Supply voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[\frac{Iout_n(@V_{DD} = 5.5V) - Iout_n(@V_{DD} = 3V)}{Iout_n(@V_{DD} = 3V)} \right] * \frac{100\%}{5.5V - 3V}$$

*5 IO excluded.

Electrical Characteristics (VDD = 3.3 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage "H" Level	VIH	CMOS logic level	0.7VDD	—	VDD	V
Input Voltage "L" Level	VIL	CMOS logic level	GND	—	0.3VDD	
Output Leakage Current	ILK	VOUT = 17 V	—	—	0.1	uA
Output Voltage (DO)	VOL	IOL = 1 mA	—	—	0.4	V
	VOH	IOH= 1 mA	VDD-0.4	—	—	
Output Current Skew (Channel-to-Channel) *1	dIOUT1	VOUT = 1.0 V Rrext = 0.94 KΩ	—	±1.0	±3.0	%
Output Current Skew (Chip-to-Chip) *2	dIOUT2		—	±1.0	±4.0	%
Output Current Skew (Channel-to-Channel)*1	dIOUT3	VOUT = 1.0 V Rrext = 6.4 KΩ	—	±1.5	±3.0	%
Output Current Skew (Chip-to-Chip)*2	dIOUT4			±1.5	±4.0	%
Output Voltage Regulation*3	% / VOUT	Rrext = 0.94 KΩ VOUT = 1 V ~ 3 V	—	±0.1	—	% / V
Supply Voltage Regulation*4	% / VDD	Rrext = 0.94 KΩ VDD = 3 V ~ 5.5 V	—	±0.7	±1	
Supply Current *5	$I_{DD1(off)}$	input signal is static Rrext = 3.69 KΩ all outputs turn off	—	1.6	—	
	$I_{DD2(on)}$	input signal is static Rrext = 3.69 KΩ all outputs turn on	—	2.5	—	
	$I_{DD3(off)}$	input signal is static Rrext = 0.94 KΩ all outputs turn off	—	4.5	—	
	$I_{DD4(on)}$	input signal is static Rrext = 0.94 KΩ all outputs turn on	—	5.5	—	

*1 Channel-to-channel skew is defined by the formula below:

$$\Delta(\%) = \left[\frac{Iout_n}{\frac{(Iout_0 + Iout_1 + \ldots + Iout_{15})}{16}} - 1 \right] * 100\%$$

*2 Chip-to-Chip skew is defined by the formula below:

$$\Delta(\%) = \left[\frac{\frac{(Iout_0 + Iout_1 + \ldots + Iout_{15})}{16} - (Ideal\ \ Output\ \ Current)}{(Ideal\ \ Output\ \ Current)} \right] * 100\%$$

*3 Output voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[\frac{Iout_n(@Vout_n = 3V) - Iout_n(@Vout_n = 1V)}{Iout_n(@Vout_n = 3V)} \right] * \frac{100\%}{3V - 1V}$$

*4 Supply voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[\frac{Iout_n(@V_{DD} = 5.5V) - Iout_n(@V_{DD} = 3V)}{Iout_n(@V_{DD} = 3V)} \right] * \frac{100\%}{5.5V - 3V}$$

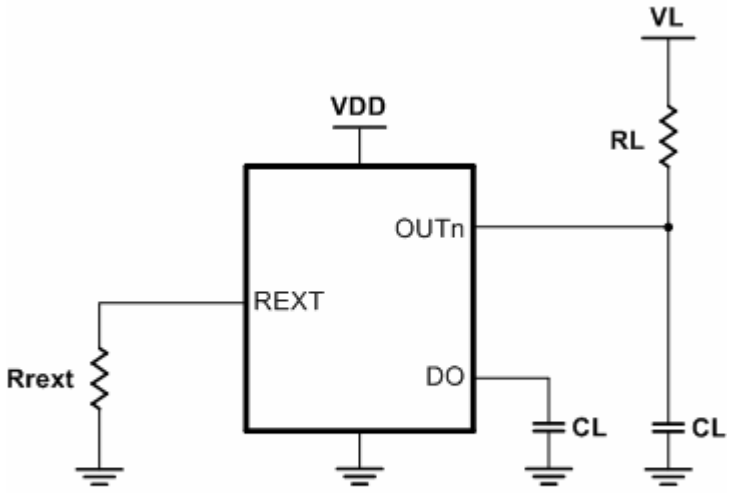
*5 IO excluded.

Switching Characteristics (VDD = 5.0V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay ('L to 'H')	PDM-to-OUT0	tpLH1	VIH = VDD VIL = GND Rrext = 1820 Ω VL =5.0 V RL = 330 Ω CL = 13 pF	—	—	—	ns
	DCK-DO	tpLH3		—	24	—	
Propagation Delay ('H' to 'L')	PDM-to-OUT0	tpHL1		—	—	—	
	DCK-DO	tpHL3		—	24	—	
Pulse Duration	PDM	$tw_{(ENB)}$		80	—	—	
	LAT	$tw_{(LAT)}$		20	—	—	
	DCK	$tw_{(DCK)}$		15	—	—	
Setup Time	LAT	$tsu_{(LAT)}$		5	—	—	
	DI	$tsu_{(D)}$		3	—	—	
Hold Time	LAT	$th_{(LAT)}$		20	—	—	
	DI	$th_{(D)}$		4	—	—	
DO Rise Time		$tr_{(DO)}$		—	15	—	
DO Fall Time		$tf_{(DO)}$		—	15	—	
Output Voltage Rise Time (turn-off)		tor		—	35	—	
Output Voltage Fall Time (turn-on)		tof		—	35	—	

Switching Characteristics (VDD = 3.3V, Ta = 25°C unless otherwise noted)

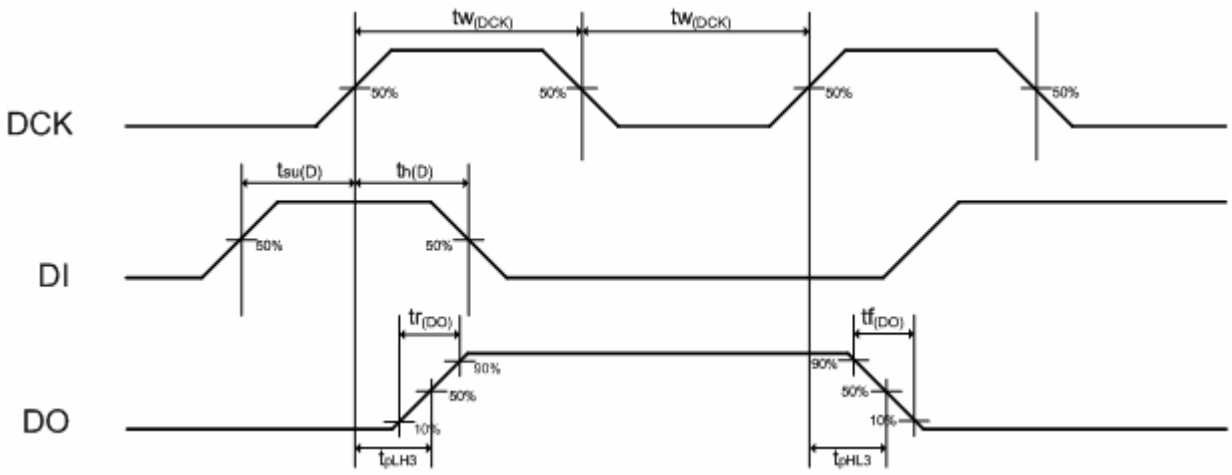
CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay ('L to 'H')	PDM-to-OUT0	tpLH1	VIH = VDD VIL = GND Rrext = 1820 Ω VL =5.0 V RL = 330 Ω CL = 13 pF	—	—	—	ns
	DCK-to-DO	tpLH3		—	35	—	
Propagation Delay ('H' to 'L')	PDM-to-OUT0	tpHL1		—	—	—	
	DCK-DO	tpHL3		—	35	—	
Pulse Duration	PDM	$tw_{(ENB)}$		120	—	—	
	LAT	$tw_{(LAT)}$		20	—	—	
	DCK	$tw_{(DCK)}$		15	—	—	
Setup Time	LAT	$tsu_{(LAT)}$		5	—	—	
	DI	$tsu_{(D)}$		3	—	—	
Hold Time	LAT	$th_{(LAT)}$		20	—	—	
	DI	$th_{(D)}$		4	—	—	
DO Rise Time		$tr_{(DO)}$		—	20	—	
DO Fall Time		$tf_{(DO)}$		—	20	—	
Output Voltage Rise Time (turn-off)		tor		—	55	—	
Output Voltage Fall Time (turn-on)		tof		—	50	—	



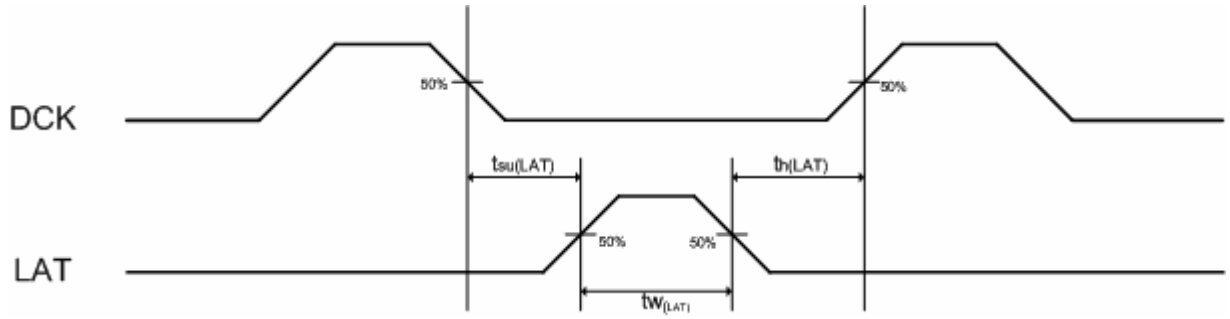
Switching Characteristics Test Circuit

Timing Diagram

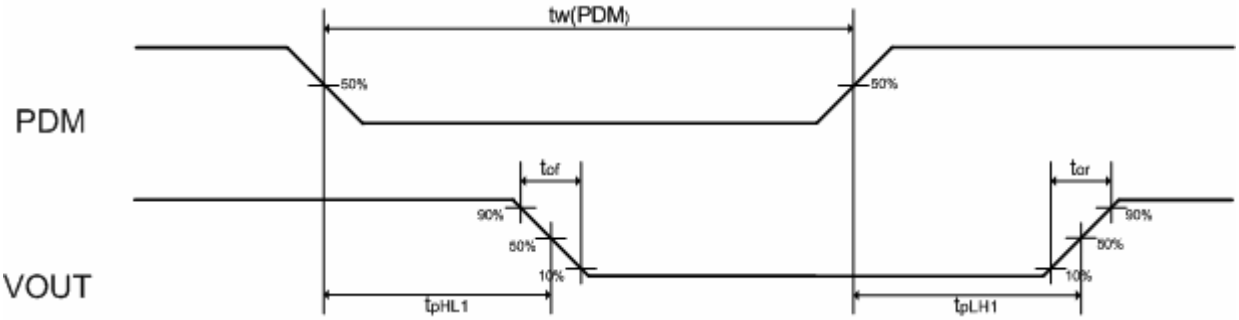
1. DCK-DI, DO



2. DCK-LAT

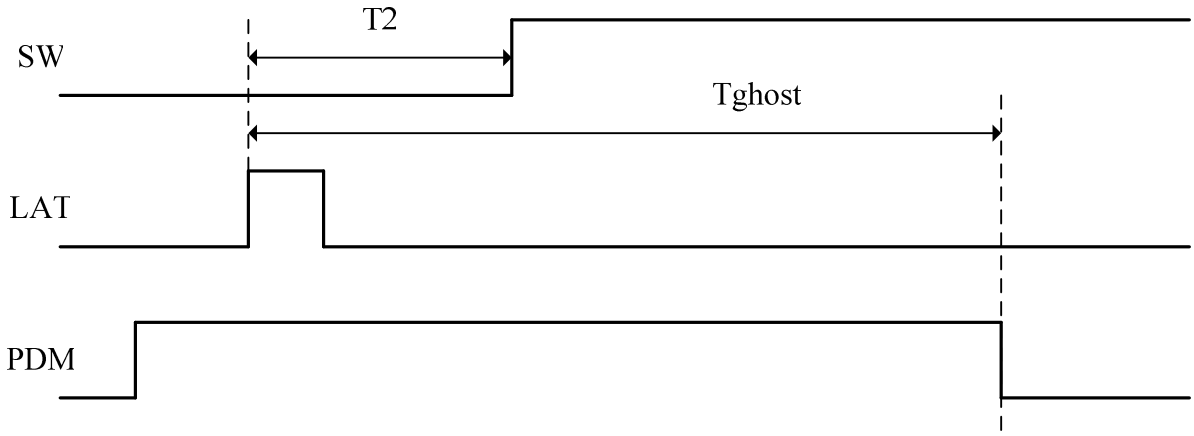


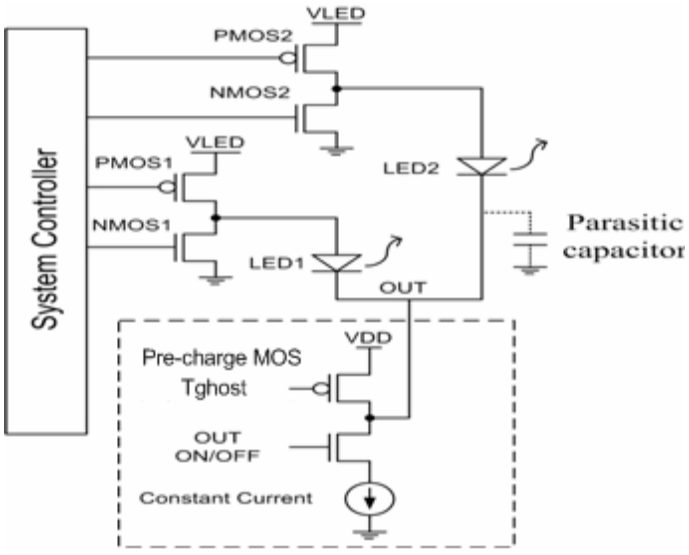
3. PDM-VOUT



Ghost Image Abatement

MY9868A provides internal pre-charge circuit to reduce ghost phenomenon of multiplexing display due to parasitic capacitors. When PDM=high, the voltage of output channels will be pulled high from the rising edge of LAT signal to the falling edge of PDM signal (Tghost), so the reverse bias would only happened in Tghost. Such design can prevent LED damage due to the reverse bias for long time. In Tghost, the high voltage on the parasitic capacitor prevents the inrush current resulting from turning on the switching PMOS of next scan line. (It is recommended to let Tghost ≧ 2000ns, where SW signal is the multiplexing switch signal.)

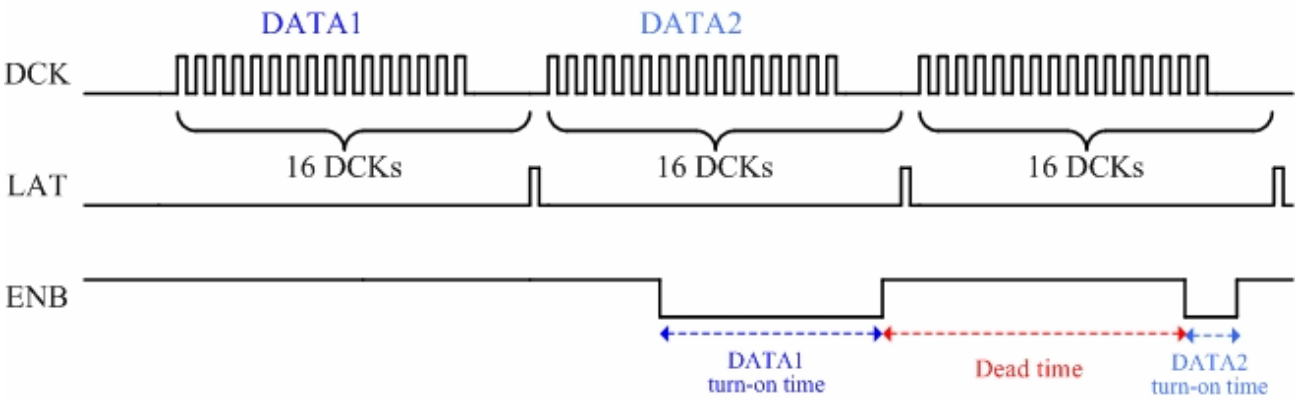




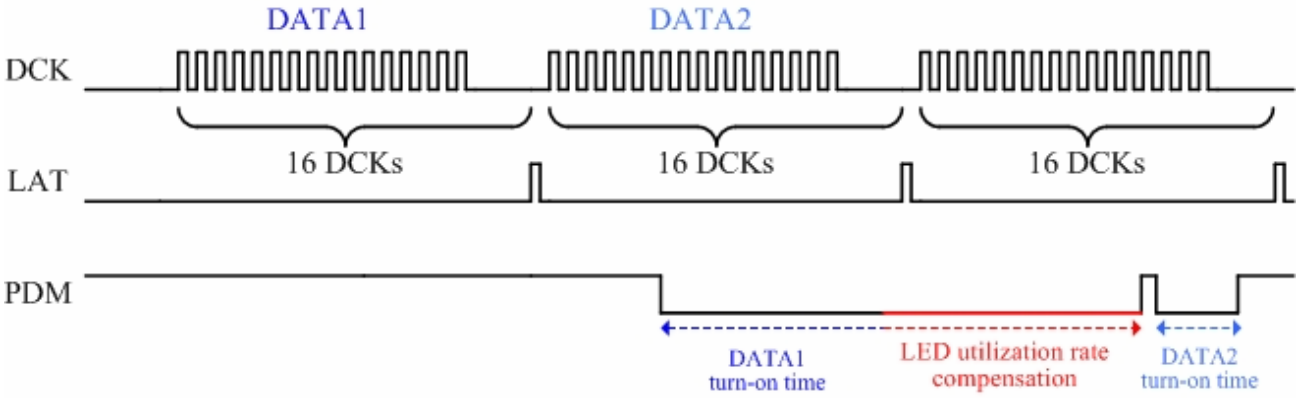
Double Latch Display Technology

MY9868A adopts the new double latch display technology to enhance display effectiveness. By saving an extra bit, MY9868A could receive a control pattern that an PDM signal extends over a LAT signal. The visual refresh rate, the LED utilization rate, the grayscale level and the low grayscale uniformity would be better than conventional pure drivers.

<Convention>



< Double latch technology>



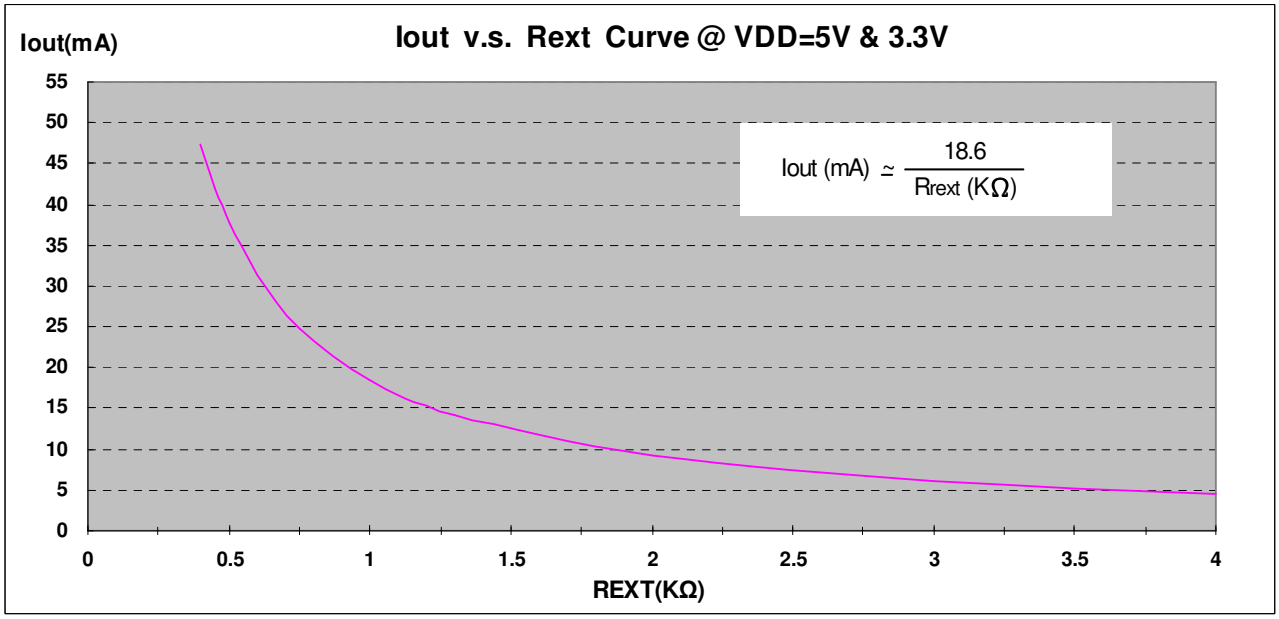
Reference Resistor

The constant current values are determined by an external resistor placed between REXT pin and GND pin. The following formula is utilized to calculate the current value:

$$Iout(mA) = \frac{18.6}{Rrext \quad (K\Omega)}$$

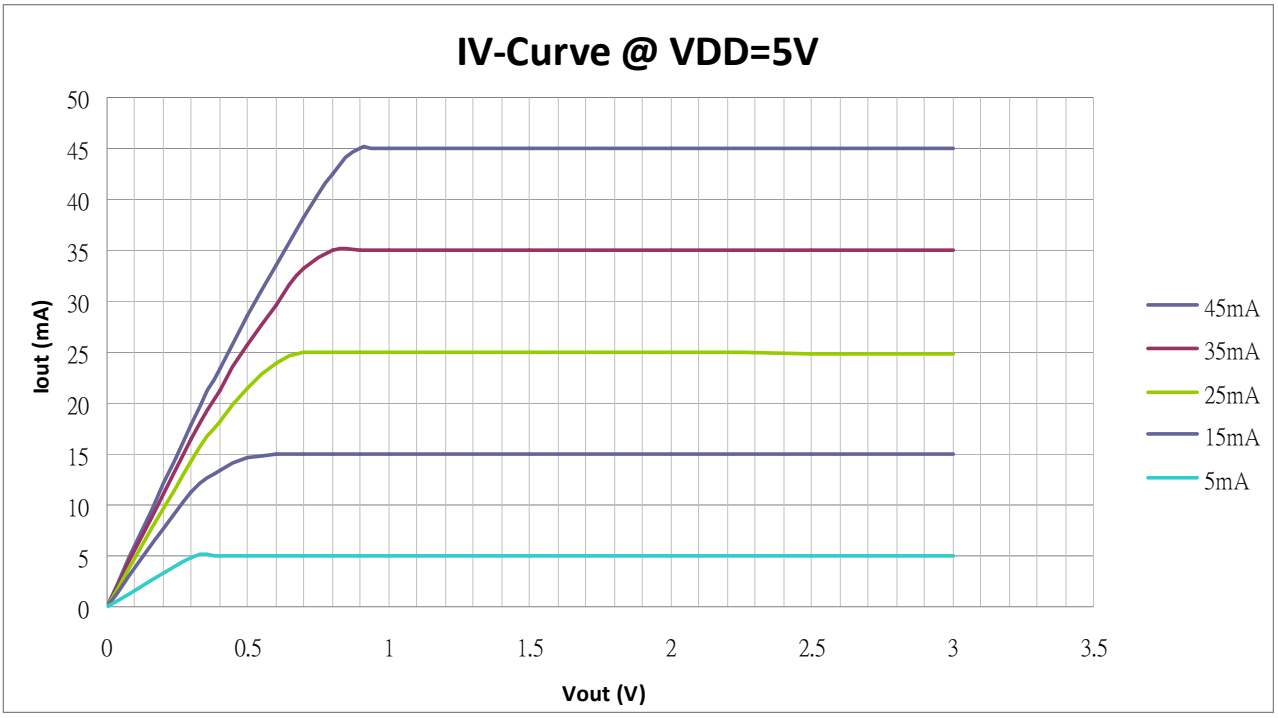
Where Rrext is a resistor placed between REXT and GND

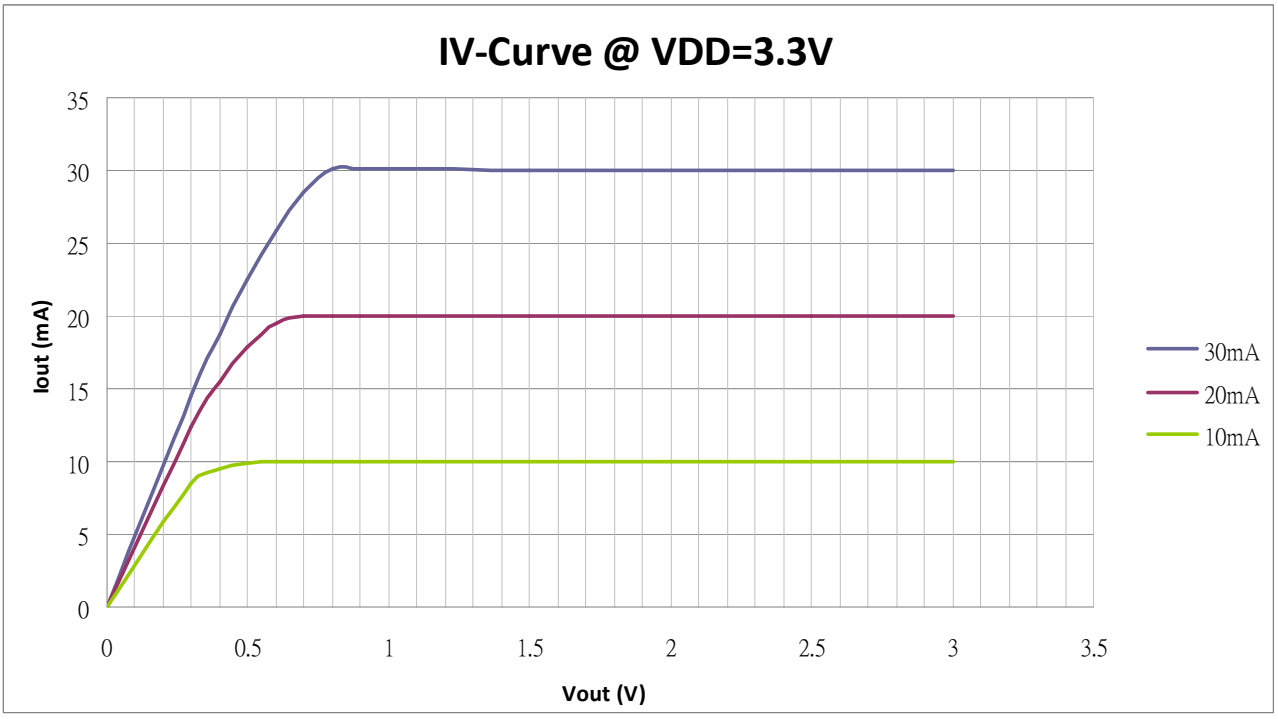
For example, Iout is 20mA when Rrext=930Ω and Iout is 5mA when Rrext=3.7KΩ



Constant-Current Output

The current characteristics could maintain invariable in the influence of loading voltage. Therefore, the MY9868A could minimize the interference of different LED forward voltages and produce the constant current. The following figures illustrate the suitable output voltage should be determined in order to keep an excellent performance.





Power Dissipation

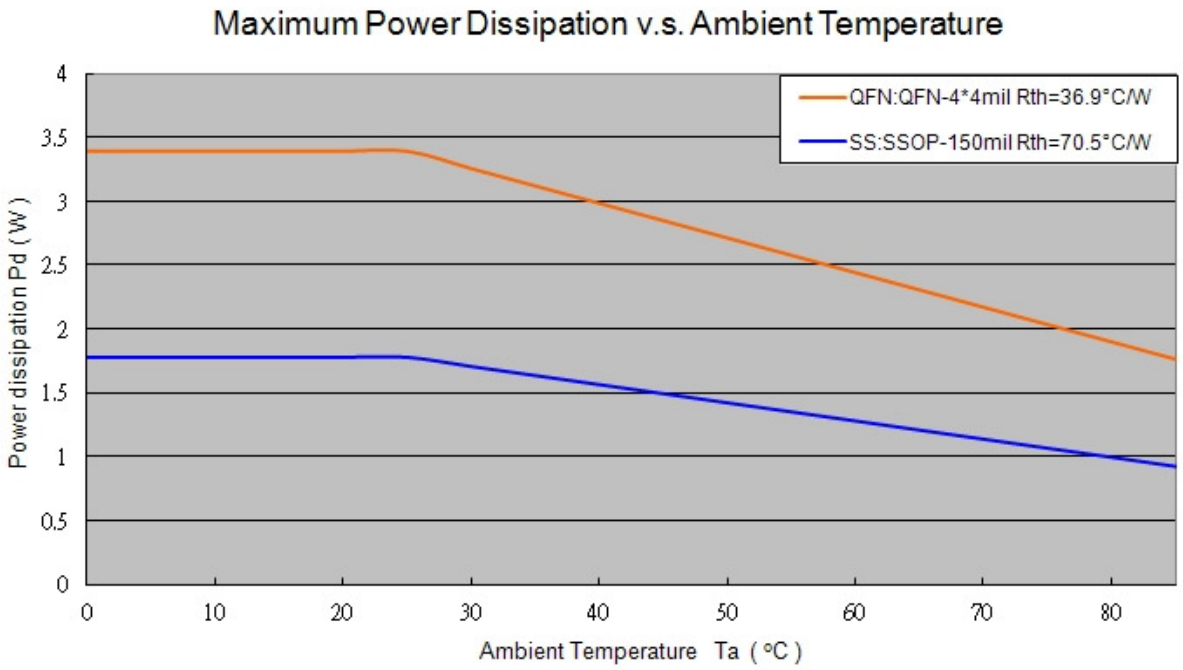
When the 16 output channels are turned on, the practical power dissipation is determined by the following equation:

$$PD\ (practical) = V_{DD} \times I_{DD} + Vout_{(0,} \times Iout_{(0,} \times Duty_{(0,} + \cdots + Vout_{(N,} \times Iout_{(N,} \times Duty_{(N,}\ ,\ where\ N=1\ to\ 15$$

In secure operating conditions, the power consumption of an integrated chip should be less than the maximum permissible power dissipation which is determined by the package types and ambient temperature. The formula for maximum power dissipation is described as follows:

$$PD\ (max) = \frac{Tj(max)(℃) - Ta(℃)}{Rth(j\text{-}a)(℃/Watt)}$$

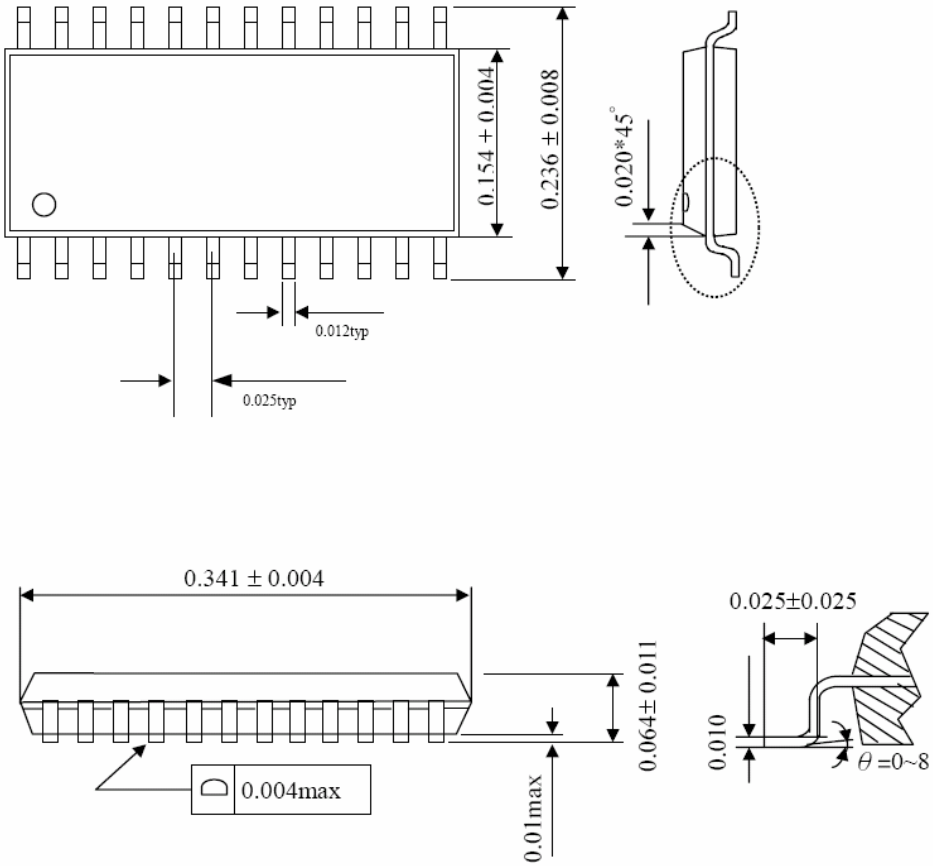
The PD(max) declines as the ambient temperature raises. Therefore, suitable operating conditions should be designed with caution according to the chosen package and the ambient temperature. The following figure illustrates the relation between the maximum power dissipation and the ambient temperature in these two different packages.



Package Outline Dimension

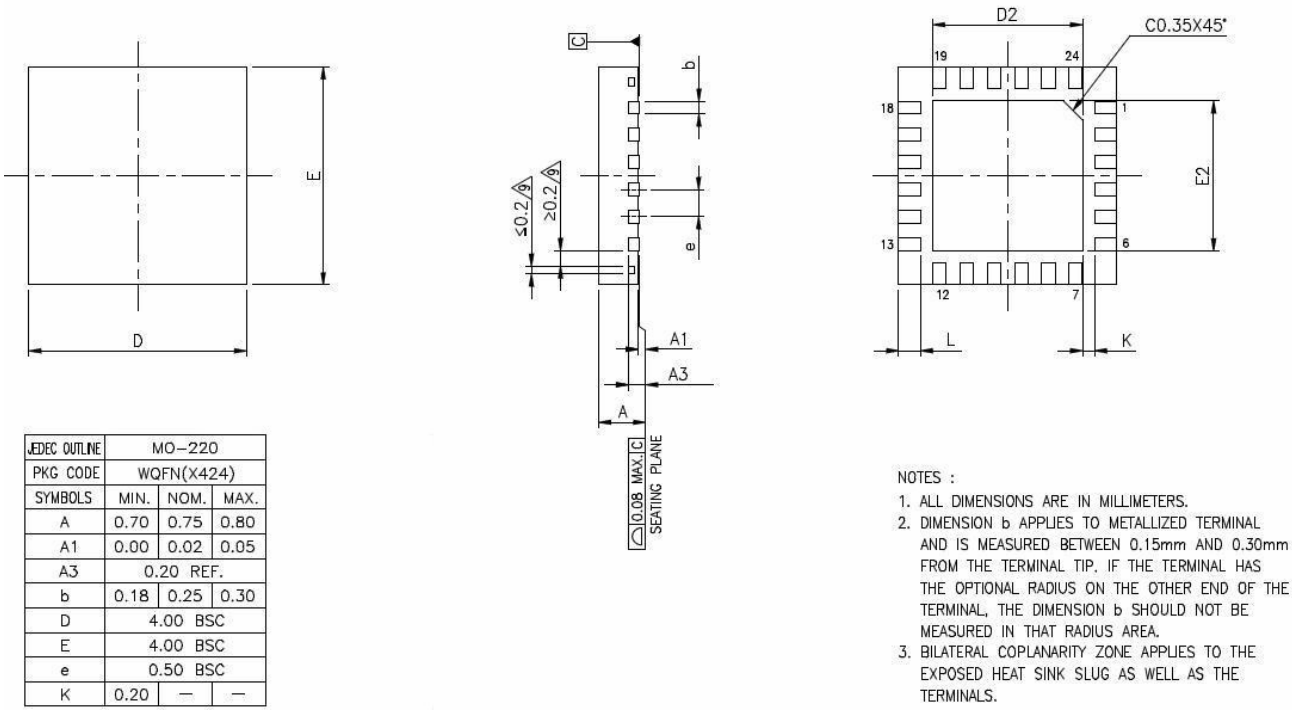
SSOP-150mil-0.635mm

Unit: inch



Package Outline Dimension

QFN24-4mm x 4mm



JEDEC OUTLINE	MO-220		
PKG CODE	WQFN(X424)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF.		
b	0.18	0.25	0.30
D	4.00 BSC		
E	4.00 BSC		
e	0.50 BSC		
K	0.20	—	—

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

E2			D2			L			LEAD FINISH		JEDEC CODE
MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
2.40	2.50	2.55	2.40	2.50	2.55	0.35	0.40	0.45	V	X	W(V)GGD-8

The products listed herein are designed for ordinary electronic applications, such as electrical appliances, audio-visual equipment, communications devices and so on. Hence, it is advisable that the devices should not be used in medical instruments, surgical implants, aerospace machinery, nuclear power control systems, disaster/crime-prevention equipment and the like. Misusing those products may directly or indirectly endanger human life, or cause injury and property loss.
MY-Semi Inc. will not take any responsibilities regarding the misusage of the products mentioned above. Anyone who purchases any products described herein with the above-mentioned intention or with such misused applications should accept full responsibility and indemnify. MY-Semi Inc. and its distributors and all their officers and employees shall defend jointly and severally against any and all claims and litigation and all damages, cost and expenses associated with such intention and manipulation.